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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,091	10/23/2003	Eric Hung	5201-27500	7976

7590 02/09/2005

Leo Peters
LSI Logic Corporation
MS D-106
1621 Barber Lane
Milpitas, CA 95035

EXAMINER	
NGUYEN, DANG T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/692,091	HUNG ET AL.	
	Examiner	Art Unit	
	Dang T Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-20* is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/26/04*.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☒ Other: *Search history*.

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed on October 23, 2003 and the Information Disclosure Statement filed on April 26, 2004.

2. Claims 1 – 20 are pending in this case. Claims 1, 8, and 17 are independent claims.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 - 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Chu et al., U.S. patent No. 5,856,937 – filed Jun. 23, 1997.

Regarding independent claim 1, Fig. 1 of Chu et al. discloses a memory module, comprising:

a printed circuit board [10] (Col. 1 lines 50-51) having opposing first ([FRONT SIDE] and chips [12] mounted to the front surface) and second outside surfaces ([BACK SIDE] and chips 18 mounted to the back surface) (Col. 2 lines 7-12);

a via extending through the printed circuit board (Col. 2 line 47) and coupled between a primary conductor on the first outside surface and a secondary conductor on the second outside surface (Col. 5 lines 31-34);

at least one primary semiconductor memory device (Figs. 2-4 [40]) arranged upon the first outside surface (Fig. 1 [FRONT SIDE]) and coupled to the primary

conductor (Fig. 5 [74]); a memory controller (Figs. 2 and 3 [19]) coupled to the primary conductor (Figs. 5 and 6 [74]); and

at least one secondary semiconductor memory device (Figs. 2-4 [20]) arranged upon the second outside surface (Fig. 1 [BACK SIDE]) substantially opposite the primary semiconductor memory device (Fig. 3) and coupled to the secondary conductor (Fig. 6 [72]).

Regarding dependent claim 2, Figs. 3 and 6 of Chu et al. disclose wherein the primary [40] and secondary [20] semiconductor memory devices each comprise a midpoint between outer lateral edges of each respective primary and secondary semiconductor memory device (see fig. 3) through which a single axis extends substantially perpendicular to the first and second outside surfaces (Fig. 6 [10'] multi-layer printed-circuit board).

Regarding dependent claim 3, Figs. 3 and 4 of Chu et al. disclose wherein the primary [40] and secondary [20] semiconductor memory devices each comprise outer lateral edges that are directly opposite the printed circuit board from each other (Col. 7 lines 33-38).

Regarding dependent claim 4, Fig. 2 of Chu et al. discloses wherein the at least one primary semiconductor memory device comprises a pair of primary semiconductor memory devices [40 and 42] and arranged on a first portion of the first outside surface [FRONT SIDE], and wherein the at least one secondary semiconductor memory device [20 and 22] comprises a pair of secondary semiconductor memory devices arranged on a second portion of the second outside surface [BACK SIDE]

substantially opposite the first portion (Figs. 3 and 4, Col. 7 lines 33-38) and (Col. 12 lines 1-6).

Regarding dependent claim 5, Figs. 3 and 6 of Chu et al. discloses wherein a first one of the pair of primary semiconductor memory devices [40] and a first one of the pair of secondary semiconductor memory devices [20] comprise a first central point through which a first axis (Fig. 3) extends substantially perpendicular to the first and second outside surfaces (Fig. 6 [substrate 10', multi-layer printed-circuit board]); and wherein a second one of the pair of primary semiconductor memory devices [42] and a second one of the pair of secondary semiconductor memory devices [22] comprise a second central point through which a second axis (Fig. 3) extends a parallel, spaced distance from the first axis (Fig. 3) substantially perpendicular to the first and second outside surfaces (Fig. 6 [substrate 10', multi-layer printed-circuit board]).

Regarding dependent claim 6, Fig. 6 of Chu et al. discloses wherein the printed circuit board [10'] further comprises:

a power supply conductor [76] arranged upon a power supply plane dielectrically spaced between the first and second outside surfaces (Col. 8 line 50 – Col. 9 line 23); and

a ground supply conductor [78] arranged upon a ground supply plane dielectrically spaced between the first and second outside surfaces [10'] and also between the power supply plane [76] and either the first outside surface or the second outside surface (Col. 8 line 50 – Col. 9 line 23).

Regarding dependent claim 7, Fig. 6 of Chu et al. discloses wherein the printed circuit board consists of four conductive layers dielectrically separated from each other,

and wherein two of the four conductive layers [74 and 72] are on the first and second outside surfaces [10'] (Col. 9 lines 11-13).

Allowable Subject Matter

4. Claims 8 - 20 are allowed.

5. The following is an examiner's statement of reasons for allowance:

With respect to claim 8, in addition to other elements in the respective claim, the prior art does not teach or suggest "a primary synchronous dynamic random access memory (SDRAM) packaged integrated circuit placed in a first slot on a first one of the opposed outside surfaces and coupled to a subset of the plurality of primary conductors; a secondary synchronous dynamic random access memory (SDRAM) packaged integrated circuit placed in a second slot on a second one of the opposed outside surfaces and coupled to a subset of the plurality of secondary conductors; and wherein the first and second slots comprise bonding pads arranged on a portion of the respective first and second ones of the opposed outside surfaces to form a footprint in which the primary SDRAM is surface mounted substantially directly opposite the secondary SDRAM".

With respect to claim 17, in addition to other elements in the respective claim, the prior art does not teach or suggest "surfacing mounting at least one lead extending from a first one of the pair of memory devices to a first end of a via extending perpendicularly through the printed circuit board and to a first end of a conductor extending across a first one of the opposing outside surfaces; surface mounting at least one lead extending from the memory controller to a second opposed end of the

conductor; and surface mounting at least one lead extending from a second one of the pair of memory devices to a second end of the via opposite the first end of the via".

Prior art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fan et al.	Patent No. US 6,381,164 B1	Date of Patent: Apr. 30, 2002
Akira et al.	PUB-NO.: JP02000031614A	PUBN-DATE: Jan. 28, 2000
Testa	Patent No.: 5,260,892	Date of Patent: Nov. 9, 1993

Contact Information

7. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 1/26/2005

RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800